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What is claimed:

1. A computer processor having control and data processing capabilities comprising:

a decode unit for decoding instructions;

a data processing facility comprising a first data execution path including fixed operators and a second data execution path including at least configurable operators, said configurable operators having a plurality of predefined configurations, at least some of which are selectable by means of an opcode portion of a data processing instruction;

wherein said decode unit is operable to detect whether a data processing instruction defines a fixed data processing operation or a configurable data processing operation, said decode unit causing the computer system to supply data for processing to said first data execution path when a fixed data processing instruction is detected and to said configurable data execution path when a configurable data processing instruction is detected.

2. A computer processor according to claim 1, wherein the decode unit is capable of decoding a stream of instruction packets from memory, each packet comprising a plurality of instructions.

3. A computer processor according to claim 1, wherein the decode unit is operable to detect if an instruction packet contains a data processing instruction.

4. A computer processor according to claim 1, wherein the configurable operators are configurable at the level of multibit values.

5. A computer processor according to claim 4, wherein the configurable operators are configurable at the level of multibit values comprising four or more bits.

6. A computer system according to claim 4, wherein the configurable operators are configurable at the level of words.

7. A computer processor according to claim 1, wherein a plurality of the fixed operators of the first data execution path is arranged to perform a plurality of fixed operations in independent lanes according to single instruction multiple data principles.

8. A computer processor according to claim 1, wherein a plurality of configurable operators of the second data execution path is arranged to perform multiple operations in different lanes according to single instruction multiple data principles.

9. A computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations performed.

10. A computer processor according to claim 9, wherein configurable operators of the second execution path are arranged to receive configuration information which determines the nature of the operations performed from a field of an instruction defining a configurable data processing operation.

11. A computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive configuration information comprising information controlling relative interconnectivity.

12. A computer processor according to any of claim 9, comprising a control map associated with configurable operators of the second data execution path, said control map being operable to receive at least one configuration bit from a configurable data processing instruction and to provide configuration information to the configurable operators responsive thereto.

13. A computer processor according to claim 12, wherein said configuration information controls interconnectivity between two or more of said configurable operators.

14. A computer processor according to claim 1, wherein configurable operators of the second execution path are arranged to receive either configuration information determining the nature of an operation to be performed or configuration information controlling interconnectivity from a source other than a configurable data processing instruction.

15. A computer processor according to claim 1, wherein at least one configurable operator of the second data execution path is capable of executing data processing instructions with an execution depth greater than two computations before returning results to a results store.

16. A computer processor according to claim 1, comprising a switch mechanism for receiving data processing operands from a configurable data processing instruction and switching them as appropriate for supply to one or more of said configurable operators.

17. A computer processor according to claim 1, comprising a switch mechanism for receiving results from one or more of said configurable operators and switching the results as appropriate for supply to one or more of a result store and feed back loop.

18. A computer processor according to claim 1, comprising a plurality of control maps for mapping configuration bits received from configurable data processing instructions to configuration information for supply to configurable operators of the second data execution path.

19. A computer processor according to claim 1, comprising a switch mechanism for receiving configuration information from a control map and switching it as appropriate for supply to configurable operators of the second data execution path.

20. A computer processor according to claim 1, comprising configurable operators selected from one or more of: multiply accumulate operators; arithmetic operators; state operators; and cross-lane permuters.

21. A computer processor according to claim 1, comprising operators and an instruction set capable of performing one or more operations selected from: Fast Fourier Transforms; Inverse Fast Fourier Transforms; Viterbi encoding/decoding; Turbo encoding/decoding; and Finite Impulse Response calculations; and any other Correlations or Convolutions.

22. A method of operating a computer processor having control and data processing capabilities, said computer processor comprising a first data execution path including fixed operators and a second data execution path including configurable operators, said configurable operators having a plurality of predefined configurations, at least some of which are selectable by means of an opcode portion of a data processing instruction, the method comprising:

decoding a plurality of instructions to detect whether at least one data processing instruction, of said plurality of instructions, defines a fixed data processing operation or a configurable data processing operation;

causing the computer processor to supply data for processing to said first data execution path when a fixed data processing instruction is detected and to said configurable data execution path when a configurable data processing instruction is detected; and

outputting the results.

23. A computer program product comprising program code means for causing a computer processor, said computer processor comprising a first data execution path including fixed operators and a second data execution path including configurable operators, said configurable operators having a plurality of predefined configurations, at least some of which are selectable by means of an opcode portion of a data processing instruction, to:

decode a plurality of instructions to detect whether at least one data processing instruction, of said plurality of instructions, defines a fixed data processing operation or a configurable data processing operation;

cause the computer processor to supply data for processing to said first data execution path when a fixed data processing instruction is detected and to said configurable data execution path when a configurable data processing instruction is detected; and

output the results.

24. A data processing instruction set comprising a first plurality instructions having a field indicating a fixed type of data processing operation and a second plurality of instructions having a field indicating a configurable type of data processing operations.

25. A computer processor having a data execution path comprising configurable operators, wherein the configurable operators comprise a plurality of pre-defined groups of operator configurations, each group comprising operators from a separate operator class.

26. A computer processor according to claim 25, wherein the operator classes comprise classes selected from one or more of: multiply accumulate operators; arithmetic operators; state operators; and permuters.

27. A computer processor according to claim 25, wherein connections between operators selected from within each of the pre-defined groups of operator configurations are capable of being configured by an opcode portion within an instruction executed by the computer processor.

28. A computer processor according to claim 25, wherein connections between operators selected from more than one of the pre-defined groups of operator

configurations are capable of being configured by an opcode portion within an instruction executed by the computer processor.